What is Claimed is:

1. A nonvolatile memory cell comprising:

a floating gate MOS transistor including:

a semiconductor body having a doping of a first type;

first and second semiconductor regions having a doping of a second type, said first and second semiconductor regions spaced apart to form a channel region in between said first and second semiconductor regions in said semiconductor body;

a floating gate disposed above said channel region in said semiconductor body;

a floating gate dielectric disposed between said floating gate and said semiconductor body; and

a tunneling hole injector including:

a conducting injector electrode from which holes are emitted;

a grid insulator disposed adjacent to said conducting injector electrode;

a grid electrode disposed adjacent to said grid insulator; and

a retention insulator disposed adjacent to said grid electrode,

wherein said grid insulator comprises an oxygen-containing material.

2. A nonvolatile memory cell in accordance with claim 1, wherein said oxygen-containing material comprises Si O_x N_y with an oxide fraction of less than about 77%.

3. A nonvolatile memory cell in accordance with claim 1, wherein said conducting injection electrode comprises p+ doped silicon and said grid electrode comprises p+ doped silicon.

4. A nonvolatile memory cell in accordance with claim 3, wherein said oxygen-containing material comprises Si O_x N_y with an oxide fraction of less than about 77%.

5. A nonvolatile memory cell in accordance with claim 3, wherein said oxygen-containing material comprises a metal oxide.

6. A nonvolatile memory cell in accordance with claim 3, wherein said oxygen-containing material comprises one or more compounds selected from the group consisting of: BeO, MgO, ZrO_2, CaO, SrO, Y_2O_3, Pr_2O_3, ThO_2, ZrO_2 and Al_2O_3.

7. A nonvolatile memory cell in accordance with claim 1, wherein said floating gate is disposed adjacent to said retention insulator and said retention insulator has a first band gap in a first portion of said retention insulator disposed adjacent to said grid electrode and a second, greater band gap in a second portion of said retention insulator disposed between said grid electrode and said floating gate.

8. A nonvolatile memory cell in accordance with claim 2, wherein said floating gate is disposed adjacent to said retention insulator and said retention insulator has a first band gap

in a first portion of said retention insulator disposed adjacent to said grid electrode and a second, greater band gap in a second portion of said retention insulator disposed between said grid electrode and said floating gate.

9. A nonvolatile memory cell in accordance with claim 3, wherein said floating gate is disposed adjacent to said retention insulator and said retention insulator has a first band gap in a first portion of said retention insulator disposed adjacent to said grid electrode and a second, greater band gap in a second portion of said retention insulator disposed between said grid electrode and said floating gate.

10. A nonvolatile memory cell in accordance with claim 4, wherein said floating gate is disposed adjacent to said retention insulator and said retention insulator has a first band gap in a first portion of said retention insulator disposed adjacent to said grid electrode and a second, greater band gap in a second portion of said retention insulator disposed between said grid electrode and said floating gate.

11. A nonvolatile memory cell in accordance with claim 5, wherein said floating gate is disposed adjacent to said retention insulator and said retention insulator has a first band gap in a first portion of said retention insulator disposed adjacent to said grid electrode and a second, greater band gap in a second portion of said retention insulator disposed between said grid electrode and said floating gate.

12. A nonvolatile memory cell in accordance with claim 6, wherein said floating gate is disposed adjacent to said retention insulator and said retention insulator has a first band gap in a first portion of said retention insulator disposed adjacent to said grid electrode and a second, greater band gap in a second portion of said retention insulator disposed between said grid electrode and said floating gate.

13. A nonvolatile memory cell as in claim 1, wherein said floating gate comprises polysilicon.

14. A nonvolatile memory cell in accordance with claim 1, wherein said retention insulator is formed of a layer of silicon oxide having a thickness in a range of about 8 nm to about 50 nm.

15. A nonvolatile memory cell in accordance with claim 1, wherein said grid electrode is thin enough to minimize loss of energy of injected charge carriers and thick enough to conduct away charge carriers that lose energy and are thermalized in said grid electrode.

16. A nonvolatile memory cell in accordance with claim 1, wherein said grid electrode has a thickness in a range of about 10 nm to about 50 nm.

17. A nonvolatile memory cell in accordance with claim 1, wherein said grid insulator has a thickness through which charge carriers will tunnel with application across said grid insulator of a bias in a range of about 2 V to about 6 V.

18. A nonvolatile memory cell in accordance with claim 1, wherein the application of a positive bias from said conducting injector electrode with respect to said grid electrode will result in holes tunneling from said conducting injector electrode to said grid electrode.

19. A nonvolatile memory cell in accordance with claim 1, wherein application of a positive bias from said conducting injector electrode with respect to said grid electrode lowers a fermi level of said conducting injector electrode to cause holes to tunnel into said grid electrode with enough energy to pass into a valence band of said retention insulator.

20. A nonvolatile memory cell comprising:

a floating gate MOS transistor including:

a semiconductor body having a doping of a first type;

first and second semiconductor regions having a doping of a second type, said first and second semiconductor regions spaced apart to form a channel region in between said first and second semiconductor regions in said semiconductor body;

a floating gate disposed above said channel region in said semiconductor body; and

a floating gate dielectric disposed between said floating gate and said semiconductor body;

a tunneling electron injector including:

a first conducting injector electrode from which electrons are emitted;

a first grid insulator disposed adjacent to said first conducting injector electrode;

a first grid electrode disposed adjacent to said first grid insulator; and

a first retention insulator disposed adjacent to said first grid electrode,

wherein said floating gate is disposed adjacent to said first retention insulator and said first retention insulator has a first band gap in a first portion of said first retention insulator disposed adjacent to said first grid electrode, and a second, greater band gap in a second portion of said first retention insulator disposed between said first grid electrode and said floating gate;

a tunneling hole injector including:

a second conducting injector electrode from which holes are emitted;

a second grid insulator disposed adjacent to said second conducting injector electrode;

a second grid electrode disposed adjacent to said second grid insulator; and

a second retention insulator disposed adjacent to said second grid electrode,

wherein said second grid insulator comprises an oxygen-containing materials.

21. A nonvolatile memory cell in accordance with claim 20, wherein said oxygen-containing material comprises SiO_xN_y with an oxide fraction of less than about 77%.

22. A nonvolatile memory cell in accordance with claim 20, wherein said second conducting injector electrode comprises p+ doped silicon, and said second grid electrode comprises p+ doped silicon.

23. A nonvolatile memory cell in accordance with claim 22, wherein said oxygen-containing material comprises SiO_xN_y with an oxide fraction of less than about 77%.

24. A nonvolatile memory cell in accordance with claim 22, wherein said oxygen-containing material comprises a metal oxide.

25. A nonvolatile memory cell in accordance with claim 22, wherein said oxygen-containing material comprises one or more compounds selected from the group consisting of: BeO, MgO, ZrO_2, CaO, SrO, Y_2O_3, Pr_2O_3, ThO_2, ZrO_2 and Al_2O_3.

26. A nonvolatile memory cell in accordance with claim 20, wherein said floating gate is disposed adjacent to said second retention insulator and said second retention insulator has a first band gap in a first portion of said second retention insulator disposed adjacent to said second grid electrode, and a second, greater band gap in a second portion of said second retention insulator disposed between said second grid electrode and said floating gate.

27. A non volatile memory cell in accordance with claim 21, wherein said floating gate is disposed adjacent to said second retention insulator and said second retention insulator

has a first band gap in a first portion of said second retention insulator disposed adjacent to said second grid electrode, and a second, greater band gap in a second portion of said second retention insulator disposed between said second grid electrode and said floating gate.

28. A nonvolatile memory cell in accordance with claim 22, wherein said floating gate is disposed adjacent to said second retention insulator and said second retention insulator has a first band gap in a first portion of said second retention insulator disposed adjacent to said second grid electrode, and a second, greater band gap in a second portion of said second retention insulator disposed between said second grid electrode and said floating gate.

29. A nonvolatile memory cell in accordance with claim 23, wherein said floating gate is disposed adjacent to said second retention insulator and said second retention insulator has a first band gap in a first portion of said second retention insulator disposed adjacent to said second grid electrode, and a second, greater band gap in a second portion of said second retention insulator disposed between said second grid electrode and said floating gate.

30. A nonvolatile memory cell in accordance with claim 24, wherein said floating gate is disposed adjacent to said second retention insulator and said second retention insulator has a first band gap in a first portion of said second retention insulator disposed adjacent to said second grid electrode, and a second, greater band gap in a second portion of said second retention insulator disposed between said second grid electrode and said floating gate.

31. A nonvolatile memory cell in accordance with claim 25, wherein said floating gate is disposed adjacent to said second retention insulator and said second retention insulator has a first band gap in a first portion of said second retention insulator disposed adjacent to said second grid electrode, and a second, greater band gap in a second portion of said second retention insulator disposed between said second grid electrode and said floating gate.

32. A nonvolatile memory cell in accordance with claim 20, wherein said floating gate has a conduction band edge and a valence band edge similar to a conduction band edge and a valence band edge of said first conducting injector electrode.

33. A nonvolatile memory cell in accordance with claim 20, wherein said floating gate comprises polysilicon.

34. A nonvolatile memory cell in accordance with claim 20, wherein said first retention insulator comprises a layer of silicon oxide having a thickness in a range of about 8 nm to about 50 nm.

35. A nonvolatile memory cell in accordance with claim 20, wherein said first grid electrode is thin enough to minimize loss of energy of injected charge carriers and thick enough to conduct away charge carriers that lose energy and are thermalized in said first grid electrode.

36. A nonvolatile memory cell in accordance with claim 20, wherein said first grid electrode has a thickness in a range of about 10 nm to about 50 nm.

37. A nonvolatile memory cell in accordance with claim 33, wherein said first grid electrode comprises a metal having a work function with a fermi level that in a flat band condition lies in approximately the middle of a band gap of said floating gate.

38. A nonvolatile memory cell in accordance with claim 20, wherein said first grid electrode comprises a metal selected from the group consisting of: Cr, Ni, Cu, W, Al, Ti, V, Zr, Mn, Nb, Ta and n-type silicon.

39. A nonvolatile memory cell in accordance with claim 20, wherein said first grid insulator comprises a layer of silicon oxide having a thickness in a range of about 2 nm to about 6 nm.

40. A nonvolatile memory cell in accordance with claim 20, wherein said first grid insulator has a thickness through which charge carriers will tunnel with application across said first grid insulator of a bias in a range of about 2 V to about 6 V.

41. A nonvolatile memory cell in accordance with claim 20, wherein said first conducting injector electrode comprises n-type doped silicon.

42. A nonvolatile memory cell in accordance with claim 41, wherein application of a negative bias from said first conducting injector electrode with respect to said first grid electrode will result in electrons tunneling from said first conducting injector electrode to said first grid electrode.

43. A nonvolatile memory cell in accordance with claim 41, wherein application of a negative bias from said first injector electrode with respect to said first grid electrode raises a conduction band of said first conducting injector electrode above a conduction band of said first retention insulator.

44. A nonvolatile memory cell in accordance with claim 22, wherein said second retention insulator has a thickness in a range of about 8 nm to about 50 nm.

45. A nonvolatile memory cell in accordance with claim 20, wherein said second grid electrode is thin enough to minimize loss of energy of injected charge carriers and thick enough to conduct away charge carriers that lose energy and are thermalized in said second grid electrode.

46. A nonvolatile memory cell in accordance with claim 22, wherein said second grid electrode has a thickness in a range of about 10 nm to about 50 nm.

47. A nonvolatile memory cell in accordance with claim 20, wherein said second grid insulator has a thickness through which charge carriers will tunnel with application across said second grid insulator of a bias in a range of about 2 V to about 6 V.

48. A nonvolatile memory cell in accordance with claim 20, wherein application of a positive bias from said second conducting injector electrode with respect to said second grid electrode will result in holes tunneling from said second conducting injector electrode to said second grid electrode.

49. A nonvolatile memory cell in accordance with claim 20, wherein application of a positive bias from said second conducting injector electrode with respect to said second grid electrode lowers a fermi level of said second conducting injector electrode below a valence band of said second retention insulator.

50. A nonvolatile memory cell in accordance with claim 20, wherein application of a positive bias from said second conducting injector electrode with respect to said second grid electrode lowers a valence band of said second conducting injector electrode below a valence band of said second retention insulator.

51. A nonvolatile memory device comprising:

a plurality of nonvolatile memory elements arranged in a rectangular array of rows and columns, each of said plurality of nonvolatile memory elements including:

a floating gate MOS transistor having a source region and a drain region formed in a semiconductor body and spaced apart by a channel region, and a floating gate disposed above said channel region; and

a tunneling hole injector having a conducting injector electrode, a grid insulator disposed adjacent to said conducting injector electrode and comprising an oxygen-containing material, a grid electrode disposed adjacent to said grid insulator, and a retention insulator disposed adjacent to said grid electrode, wherein said floating gate is disposed adjacent to said retention insulator and said retention insulator has a first band gap in a first portion of said retention insulator disposed adjacent to said grid electrode and a second, greater band gap in a second portion of said retention insulator disposed between said grid electrode and said floating gate;

a plurality of word lines, a separate one of said plurality of word lines coupled to said control gate of each of said plurality of nonvolatile memory cells in a same row;

a plurality of bit lines, a separate one of said plurality of bit lines coupled to said drain region of each of said plurality of nonvolatile memory cells in a same column;

a plurality of source lines, at least one of said plurality of source lines coupled to said source region of each of said plurality of nonvolatile memory cells in a same row;

a plurality of injector lines, at least one of said plurality of injector lines coupled to said conducting injector electrode of each of said plurality of nonvolatile memory cells in a same row; and

a plurality of grid lines, at least one of said plurality of grid lines coupled to said grid electrode of each of said plurality of nonvolatile memory cells in a same column.

52. A nonvolatile memory device comprising:

a plurality of nonvolatile memory elements arranged in a rectangular array of rows and columns, each of said plurality of nonvolatile memory elements including:

a floating gate MOS transistor having a source region and a drain region formed in a semiconductor body and spaced apart by a channel region, and a floating gate disposed above said channel region; and

a tunneling hole injector having a conducting injector electrode and comprising an oxygen-containing material, a grid insulator disposed adjacent to said conducting injector electrode, a grid electrode disposed adjacent to said grid insulator, and a retention insulator disposed adjacent to said grid electrode, wherein said floating gate is disposed adjacent to said retention insulator and said retention insulator has a first band gap in a first portion of said retention insulator disposed adjacent to said grid electrode and a second, greater band gap in a second portion of said retention insulator disposed between said grid electrode and said floating gate;

a plurality of word lines, a separate one of said plurality of word lines coupled to said control gate of each of said plurality of nonvolatile memory cells in a same row;

a plurality of bit lines, a separate one of said plurality of bit lines coupled to said drain region of each of said plurality of nonvolatile memory cells in a same column;

a plurality of injector lines, at least one of said plurality of injector lines coupled to said conducting injector electrode of each of said plurality of nonvolatile memory cells in a same column; and

a plurality of grid lines, at least one of said plurality of grid lines coupled to said grid electrode of each of said plurality of nonvolatile memory cells in a same row.

53. A nonvolatile memory device comprising:

a plurality of nonvolatile memory elements arranged in a rectangular array of rows and columns, each of said plurality of nonvolatile memory elements including:

a floating gate MOS transistor having a source region and a drain region formed in a semiconductor body and spaced apart by a channel region, and a floating gate disposed above said channel region; and

a tunneling electron injector having a first conducting injector electrode, a first grid insulator disposed adjacent to said first conducting injector electrode, a first grid electrode disposed adjacent to said first grid insulator, and a first retention insulator disposed adjacent to said first grid electrode, wherein said floating gate is disposed adjacent to said first retention insulator and said first retention insulator has a first band gap in a first portion of said first retention insulator disposed adjacent to said first grid electrode, and a second, greater band gap in a second portion of said first retention insulator disposed between said first grid electrode and said floating gate;

a tunneling hole injector having a second conducting injector electrode, a second grid insulator disposed adjacent to said second conducting injector electrode and comprising an oxygen-containing material, a second grid electrode disposed adjacent to said second grid insulator, and a second retention insulator disposed adjacent to said second grid electrode, wherein said floating gate is disposed adjacent to said second retention

insulator and said second retention insulator has a first band gap in a first portion of said second retention insulator disposed adjacent to said second grid electrode, and a second, greater, band gap in a second portion of said second retention insulator disposed between said second grid electrode and said floating gate;

a plurality of word lines, a separate one of said plurality of word lines coupled to said control gate of each of said plurality of nonvolatile memory cells in a same row;

a plurality of bit lines, a separate one of said plurality of bit lines coupled to said drain region of each of said plurality of nonvolatile memory cells in a same column;

a plurality of source lines, at least one of said plurality of source lines coupled to said source region of each of said plurality of nonvolatile memory cells in a same row;

a first plurality of injector lines, at least one of said first plurality of injector lines coupled to said first conducting injector electrode of each of said plurality of nonvolatile memory cells in a same row;

a first plurality of grid lines, at least one of said first plurality of grid lines coupled to said first grid electrode of each of said plurality of nonvolatile memory cells in a same column;

a second plurality of injector lines, at least one of said second plurality of injector lines coupled to said second conducting injector electrode of each of said plurality of nonvolatile memory cells in a same row; and

a second plurality of grid lines, at least one of said second plurality of grid lines coupled to said second grid electrode of each of said plurality of nonvolatile memory cells in a same column.

54. A nonvolatile memory device comprising:

a plurality of nonvolatile memory elements arranged in a rectangular array of rows and columns, each of said plurality of nonvolatile memory elements including:

a floating gate MOS transistor having a source region and a drain region formed in a semiconductor body and spaced apart by a channel region, and a floating gate disposed above said channel region; and

a tunneling electron injector having a first conducting injector electrode, a first grid insulator disposed adjacent to said first conducting injector electrode, a first grid electrode disposed adjacent to said first grid insulator, and a first retention insulator disposed adjacent to said first grid electrode, wherein said floating gate is disposed adjacent to said first retention insulator and said first retention insulator has a first band gap in a first portion of said first retention insulator disposed adjacent to said first grid electrode, and a second, greater band gap in a second portion of said first retention insulator disposed between said first grid electrode and said floating gate;

a tunneling hole injector having a second conducting injector electrode, a second grid insulator disposed adjacent to said second conducting injector electrode and comprising an oxygen containing materials a second grid electrode disposed adjacent to said second grid insulator, and a second retention insulator disposed adjacent to said second grid electrode, wherein said floating gate is disposed adjacent to said second retention insulator and said second retention insulator has a first band gap in a first portion of said second retention insulator disposed adjacent to said second grid electrode, and comprising

an oxygen-containing material and a second, greater, band gap in a second portion of said second retention insulator disposed between said second grid electrode and said floating gate;

a plurality of word lines, a separate one of said plurality of word lines coupled to said control gate of each of said plurality of nonvolatile memory cells in a same row;

a plurality of bit lines, a separate one of said plurality of bit lines coupled to said drain region of each of said plurality of nonvolatile memory cells in a same column;

a first plurality of injector lines, at least one of said first plurality of injector lines coupled to said first conducting injector electrode of each of said plurality of nonvolatile memory cells in a same column; and

a first plurality of grid lines, at least one of said first plurality of grid lines coupled to said first grid electrode of each of said plurality of nonvolatile memory cells in a same row.

55. A nonvolatile memory cell in accordance with claim 1, wherein said retention insulator further comprises a third portion disposed between said first portion and said second portion, said third portion having a graded band gap.

56. A nonvolatile memory cell in accordance with claim 1, wherein said retention insulator further comprises a third portion having a continuously graded band gap disposed between said first portion and said second portion.

57. A nonvolatile memory cell in accordance with claim 1, wherein said first portion of said retention insulator comprises a film formed of silicon oxide and said second portion of said retention insulator comprises a film formed of silicon oxinitride.

58. A nonvolatile memory cell in accordance with claim 1, wherein said retention insulator comprises a continuously graded band gap structure disposed between said first portion and said second portion of said retention insulator, said structure comprising SiO_x and SiO_xN_y.

59. A nonvolatile memory cell in accordance with claim 16, further comprising:

a third portion of said first retention insulator disposed between said first portion and said second portion of said first retention insulator, said third portion of said first retention insulator having a graded band gap; and

a third portion of said second retention insulator disposed between said first portion and said second portion of said second retention insulator, said third portion of said second retention insulator having a graded band gap.

60. A nonvolatile memory cell in accordance with claim 20, further comprising:

a third portion of said first retention insulator having a continuously graded band gap disposed between said first portion and said second portion of said first retention insulator; and

a third portion of said second retention insulator having a continuously graded band gap disposed between said first portion and said second portion of said second retention insulator.

61. A nonvolatile memory cell in accordance with claim 20, wherein:

a first portion of said first retention insulator comprises a film formed of silicon oxide and said second portion of said first retention insulator comprises a film formed of silicon oxynitride; and

said first portion of said second retention insulator comprises a film formed of silicon oxide and said second portion of said second retention insulator comprises a film formed of silicon oxynitride.

62. A nonvolatile memory cell in accordance with claim 20, wherein:

said first retention insulator comprises a continuously graded band gap structure disposed between said first portion and said second portion of said first retention insulator, said structure comprising SiO_x and SiO_xN_y; and

said second retention insulator comprises a continuously graded band gap structure disposed between said first portion and said second portion of said second retention insulator, said structure comprising SiO_x and SiO_xN_y.

63. A nonvolatile memory cell in accordance with claim 51, further comprising a third portion disposed between said first portion and said second portion of said retention insulator, said third portion having a graded band gap.

64. A nonvolatile memory cell in accordance with claim 51, wherein said retention insulator further comprises a third portion having a continuously graded band gap disposed between said first portion and said second portion of said retention insulator.

65. A nonvolatile memory cell in accordance with claim 51, wherein said first portion of said retention insulator comprises a film formed of silicon oxide and said second portion of said retention insulator comprises a film formed of silicon oxynitride.

66. A nonvolatile memory cell in accordance with claim 53, wherein said retention insulator comprises a continuously graded band gap structure disposed between said first portion and said second portion of said retention insulator, said structure comprising SiO_x and SiO_xN_y.

67. A nonvolatile memory cell in accordance with claim 53, further comprising:

a third portion of said first retention insulator disposed between said first portion and said second portion of said first retention insulator, said third portion of said first retention insulator having a graded band gap; and

a third portion of said second retention insulator disposed between said first portion and said second portion of said second retention insulator, said third portion of said second retention insulator having a graded band gap.

68. A nonvolatile memory cell in accordance with claim 53, further comprising:

a third portion of said first retention insulator having a continuously graded band gap disposed between said first portion and said second portion of said first retention insulator; and

a third portion of said second retention insulator having a continuously graded band gap disposed between said first portion and said second portion of said second retention insulator.

69. A nonvolatile memory cell in accordance with claim 53, wherein:

said first portion of said first retention insulator comprises a film formed of silicon oxide and said second portion of said first retention insulator comprises a film formed of silicon oxynitride; and

said first portion of said second retention insulator comprises a film formed of silicon oxide and said second portion of said second retention insulator comprises a film formed of silicon oxynitride.

70. A nonvolatile memory cell in accordance with claim 53, wherein:

said first retention insulator comprises a continuously graded band gap structure disposed between said first portion and said second portion of said first retention insulator, said structure comprising SiO_x and SiO_xN_y; and

said second retention insulator comprises a continuously graded band gap structure disposed between said first portion and said second portion of said second retention insulator, said structure comprising SiO_x and SiO_xN_y.

71. A nonvolatile memory cell comprising:

a floating gate MOS transistor including;

a semiconductor body having a doping of a first type;

first and second semiconductor regions having a doping of a second type, said first and second semiconductor regions spaced apart to form a channel region in between said first and second semiconductor regions in said semiconductor body;

a floating gate disposed above said channel region in said semiconductor body;

a floating gate dielectric disposed between said floating gate and said semiconductor body; and

a tunneling hole injector including:

a conducting injector electrode from which holes are emitted;

a grid insulator disposed adjacent to said conducting injector electrode;

a grid electrode disposed adjacent to said grid insulator; and

a retention insulator disposed adjacent to said grid electrode,

wherein charge carriers are ballistically injected from said charge injector through said retention insulator to said floating gate.

72. A nonvolatile memory cell comprising:

a floating gate MOS transistor including;

a semiconductor body having a doping of a first type;

first and second semiconductor regions having a doping of a second type, said first and second semiconductor regions spaced apart to form a channel region in between said first and second semiconductor regions in said semiconductor body;

a floating gate disposed above said channel region in said semiconductor body;

a floating gate dielectric disposed between said floating gate and said semiconductor body; and

a tunneling hole injector including:

a conducting injector electrode from which holes are emitted;

a grid insulator disposed adjacent to said conducting injector electrode;

a grid electrode disposed adjacent to said grid insulator; and

a retention insulator disposed adjacent to said grid electrode,

wherein charge carriers are ballistically injected from said charge injector through said retention insulator to said floating gate.

73. A nonvolatile memory cell comprising:

a floating gate MOS transistor including:

a semiconductor body having a doping of a first type;

first and second semiconductor regions having a doping of a second type, said first and second semiconductor regions spaced apart to form a channel region in between said first and second semiconductor regions in said semiconductor body;

a floating gate disposed above said channel region in said semiconductor body; and

a floating gate dielectric disposed between said floating gate and said semiconductor body;

a tunneling electron injector including:

a first conducting injector electrode from which electrons are emitted;

a first grid insulator disposed adjacent to said first conducting injector electrode;

a first grid electrode disposed adjacent to said first grid insulator; and

a first retention insulator disposed adjacent to said first grid electrode,

wherein said floating gate is disposed adjacent to said first retention insulator and said first retention insulator has a first band gap in a first portion of said first retention insulator disposed adjacent to said first grid electrode, and a second, greater band gap in a second portion of said first retention insulator disposed between said first grid electrode and said floating gate;

a tunneling hole injector including:

a second conducting injector electrode from which holes are emitted;

a second grid insulator disposed adjacent to said second conducting injector electrode;

a second grid electrode disposed adjacent to said second grid insulator; and

a second retention insulator disposed adjacent to said second grid electrode,

wherein charge carriers are ballistically injected from said respective injectors, through said respective retention insulators to said floating gate.

74. A nonvolatile memory cell comprising:

a floating gate MOS transistor including:

a semiconductor body having a doping of a first type;

first and second semiconductor regions having a doping of a second type, said first and second semiconductor regions spaced apart to form a channel region in between said first and second semiconductor regions in said semiconductor body;

a floating gate disposed above said channel region in said semiconductor body; and

a floating gate dielectric disposed between said floating gate and said semiconductor body;

a tunneling electron injector including:

a first conducting injector electrode from which electrons are emitted;

a first grid insulator disposed adjacent to said first conducting injector electrode;

a first grid electrode disposed adjacent to said first grid insulator; and

a first retention insulator disposed adjacent to said first grid electrode,

wherein said floating gate is disposed adjacent to said first retention insulator and said first retention insulator has a first band gap in a first portion of said first retention insulator disposed adjacent to said first grid electrode, and a second, greater band gap in a

second portion of said first retention insulator disposed between said first grid electrode and said floating gate;

a tunneling hole injector including:

a second conducting injector electrode from which holes are emitted;

a second grid insulator disposed adjacent to said second conducting injector electrode;

a second grid electrode disposed adjacent to said second grid insulator; and

a second retention insulator disposed adjacent to said second grid electrode,

wherein said floating gate is disposed adjacent to said second retention insulator and said second retention insulator has a first band gap in a first portion of said second retention insulator disposed adjacent to said second grid electrode, and a second, greater band gap in a second portion of said second retention insulator disposed between said second grid electrode and said floating gate, and charge carriers are ballistically injected from said respective injectors, through said respective retention insulators to said floating gate.

75. A nonvolatile memory device comprising:

a plurality of nonvolatile memory elements arranged in a rectangular array of rows and columns, each of said plurality of nonvolatile memory elements including:

a floating gate MOS transistor having a source region and a drain region formed in a semiconductor body and spaced apart by a channel region, and a floating gate disposed above said channel region; and

a tunneling charge injector having a conducting injector electrode, a grid insulator disposed adjacent to said conducting injector electrode, a grid electrode disposed adjacent to said grid insulator, and a retention insulator disposed adjacent to said grid electrode, wherein said floating gate is disposed adjacent to said retention insulator and said retention insulator has a first band gap in a first portion of said retention insulator disposed adjacent to said grid electrode and a second, greater band gap in a second portion of said retention insulator disposed between said grid electrode and said floating gate;

a plurality of word lines, a separate one of said plurality of word lines coupled to said control gate of each of said plurality of nonvolatile memory cells in a same row;

a plurality of bit lines, a separate one of said plurality of bit lines coupled to said drain region of each of said plurality of nonvolatile memory cells in a same column;

a plurality of source lines, at least one of said plurality of source lines coupled to said source region of each of said plurality of nonvolatile memory cells in a same row;

a plurality of injector lines, at least one of said plurality of injector lines coupled to said conducting injector electrode of each of said plurality of nonvolatile memory cells in a same row; and

a plurality of grid lines, at least one of said plurality of grid lines coupled to said grid electrode of each of said plurality of nonvolatile memory cells in a same column,

wherein charge carriers are ballistically injected from said charge injector through said retention insulator to said floating gate.

76. A nonvolatile memory device comprising:

a plurality of nonvolatile memory elements arranged in a rectangular array of rows and columns, each of said plurality of nonvolatile memory elements including:

a floating gate MOS transistor having a source region and a drain region formed in a semiconductor body and spaced apart by a channel region, and a floating gate disposed above said channel region; and

a tunneling charge injector having a conducting injector electrode, a grid insulator disposed adjacent to said conducting injector electrode, a grid electrode disposed adjacent to said grid insulator, and a retention insulator disposed adjacent to said grid electrode, wherein said floating gate is disposed adjacent to said retention insulator and said retention insulator has a first band gap in a first portion of said retention insulator disposed adjacent to said grid electrode and a second, greater band gap in a second portion of said retention insulator disposed between said grid electrode and said floating gate;

a plurality of word lines, a separate one of said plurality of word lines coupled to said control gate of each of said plurality of nonvolatile memory cells in a same row;

a plurality of bit lines, a separate one of said plurality of bit lines coupled to said drain region of each of said plurality of nonvolatile memory cells in a same column;

a plurality of injector lines, at least one of said plurality of injector lines coupled to said conducting injector electrode of each of said plurality of nonvolatile memory cells in a same column; and

a plurality of grid lines, at least one of said plurality of grid lines coupled to said grid electrode of each of said plurality of nonvolatile memory cells in a same row.

77. A nonvolatile memory device comprising:

a plurality of nonvolatile memory elements arranged in a rectangular array of rows and columns, each of said plurality of nonvolatile memory elements including:

a floating gate MOS transistor having a source region and a drain region formed in a semiconductor body and spaced apart by a channel region, and a floating gate disposed above said channel region; and

a tunneling electron injector having a first conducting injector electrode, a first grid insulator disposed adjacent to said first conducting injector electrode, a first grid electrode disposed adjacent to said first grid insulator, and a first retention insulator disposed adjacent to said first grid electrode, wherein said floating gate is disposed adjacent to said first retention insulator and said first retention insulator has a first band gap in a first portion of said first retention insulator disposed adjacent to said first grid electrode, and a second, greater band gap in a second portion of said first retention insulator disposed between said first grid electrode and said floating gate;

a tunneling hole injector having a second conducting injector electrode, a second grid insulator disposed adjacent to said second conducting injector electrode, a second grid electrode disposed adjacent to said second grid insulator, and a second retention insulator disposed adjacent to said second grid electrode, wherein said floating gate is disposed adjacent to said second retention insulator and said second retention insulator has a first band gap in a first portion of said second retention insulator disposed adjacent to said second grid electrode, and a second, greater, band gap in a second portion of said second retention insulator disposed between said second grid electrode and said floating gate;

a plurality of word lines, a separate one of said plurality of word lines coupled to said control gate of each of said plurality of nonvolatile memory cells in a same row;

a plurality of bit lines, a separate one of said plurality of bit lines coupled to said drain region of each of said plurality of nonvolatile memory cells in a same column;

a plurality of source lines, at least one of said plurality of source lines coupled to said source region of each of said plurality of nonvolatile memory cells in a same row;

a first plurality of injector lines, at least one of said first plurality of injector lines coupled to said first conducting injector electrode of each of said plurality of nonvolatile memory cells in a same row;

a first plurality of grid lines, at least one of said first plurality of grid lines coupled to said first grid electrode of each of said plurality of nonvolatile memory cells in a same column;

a second plurality of injector lines, at least one of said second plurality of injector lines coupled to said second conducting injector electrode of each of said plurality of nonvolatile memory cells in a same row; and

a second plurality of grid lines, at least one of said second plurality of grid lines coupled to said second grid electrode of each of said plurality of nonvolatile memory cells in a same column,

wherein charge carriers are ballistically injected from said respective injectors, through said respective retention insulators to said floating gate.

78. A nonvolatile memory device comprising:

a plurality of nonvolatile memory elements arranged in a rectangular array of rows and columns, each of said plurality of nonvolatile memory elements including:

a floating gate MOS transistor having a source region and a drain region formed in a semiconductor body and spaced apart by a channel region, and a floating gate disposed above said channel region; and

a tunneling electron injector having a first conducting injector electrode, a first grid insulator disposed adjacent to said first conducting injector electrode, a first grid electrode disposed adjacent to said first grid insulator, and a first retention insulator disposed adjacent to said first grid electrode, wherein said floating gate is disposed adjacent to said first retention insulator and said first retention insulator has a first band gap in a first portion of said first retention insulator disposed adjacent to said first grid electrode, and a second, greater band gap in a second portion of said first retention insulator disposed between said first grid electrode and said floating gate;

a tunneling hole injector having a second conducting injector electrode, a second grid insulator disposed adjacent to said second conducting injector electrode, a second grid electrode disposed adjacent to said second grid insulator, and a second retention insulator disposed adjacent to said second grid electrode, wherein said floating gate is disposed adjacent to said second retention insulator and said second retention insulator has a first band gap in a first portion of said second retention insulator disposed adjacent to said second grid electrode, and comprising an oxygen-containing material and a second, greater, band gap in a second portion of said second retention insulator disposed between said second grid electrode and said floating gate;

a plurality of word lines, a separate one of said plurality of word lines coupled to said control gate of each of said plurality of nonvolatile memory cells in a same row;

a plurality of bit lines, a separate one of said plurality of bit lines coupled to said drain region of each of said plurality of nonvolatile memory cells in a same column;

a first plurality of injector lines, at least one of said first plurality of injector lines coupled to said first conducting injector electrode of each of said plurality of nonvolatile memory cells in a same column; and

a first plurality of grid lines, at least one of said first plurality of grid lines coupled to said first grid electrode of each of said plurality of nonvolatile memory cells in a same row,

wherein charge carriers are ballistically injected from said respective injectors, through said respective retention insulators to said floating gate.

CAY-006 Insert C (New claims 79 – 93)

79. A nonvolatile memory cell comprising:

a floating gate MOS transistor including:

a semiconductor body having a doping of a first type;

first and second semiconductor regions having a doping of a second type, said first and second semiconductor regions spaced apart to form a channel region in between said first and second semiconductor regions in said semiconductor body;

a floating gate disposed above said channel region in said semiconductor body;

a floating gate dielectric disposed between said floating gate and said semiconductor body;

a retention dielectric disposed over said floating gate;

a grid electrode disposed over said retention dielectric;

a tunnel dielectric disposed over said grid electrode; and

a tunneling charge injector disposed over said tunnel dielectric.

80. A nonvolatile memory cell in accordance with claim 79, wherein said first and second semiconductor regions are n+ doped.

81. A nonvolatile memory cell in accordance with claim 79, wherein said floating gate is disposed adjacent to said retention dielectric and said retention dielectric has a first band gap in a first portion of said retention dielectric disposed adjacent to said grid electrode and a second, greater band gap in a second portion of said retention dielectric disposed between said grid electrode and said floating gate.

82. A nonvolatile memory cell as in claim 79, wherein said floating gate comprises polysilicon.

83. A nonvolatile memory cell in accordance with claim 79, wherein said retention dielectric is formed of a layer of silicon oxide having a thickness in a range of about 8 nm to about 50 nm.

84. A nonvolatile memory cell in accordance with claim 79, wherein said grid electrode is thin enough to minimize loss of energy of injected charge carriers and thick enough to conduct away charge carriers that lose energy and are thermalized in said grid electrode.

85. A nonvolatile memory cell in accordance with claim 79, wherein said grid electrode has a thickness in a range of about 10 nm to about 50 nm.

86. A nonvolatile memory cell in accordance with claim 79, wherein the application of a positive bias from said injector with respect to said grid electrode will result in holes tunneling from said injector to said grid electrode.

87. A nonvolatile memory cell in accordance with claim 79, wherein application of a positive bias from said injector with respect to said grid electrode lowers a fermi level of said injector to cause holes to tunnel into said grid electrode with enough energy to pass into a valence band of said retention dielectric.

88. A nonvolatile memory device comprising:

a plurality of nonvolatile memory elements arranged in a rectangular array of rows and columns, each of said plurality of nonvolatile memory elements including:

a floating gate MOS transistor having a source region and a drain region formed in a semiconductor body and spaced apart by a channel region, and a floating gate disposed above said channel region; and

a tunneling hole injector having a conducting injector electrode, a grid electrode, a tunnel dielectric disposed between said injector and said grid, and a retention insulator disposed between said grid and said floating gate;

a plurality of bit lines, a separate one of said plurality of bit lines coupled to said drain region of each of said plurality of nonvolatile memory cells in a same column;

a plurality of source lines, at least one of said plurality of source lines coupled to said source region of each of said plurality of nonvolatile memory cells in a same row;

a plurality of injector lines, at least one of said plurality of injector lines coupled to said conducting injector electrode of each of said plurality of nonvolatile memory cells in a same row; and

a plurality of grid lines, at least one of said plurality of grid lines coupled to said grid electrode of each of said plurality of nonvolatile memory cells in a same column.

89. A nonvolatile memory device comprising:

a plurality of nonvolatile memory elements arranged in a rectangular array of rows and columns, each of said plurality of nonvolatile memory elements including:

a floating gate MOS transistor having a source region and a drain region formed in a semiconductor body and spaced apart by a channel region, and a floating gate disposed above said channel region; and

a tunneling hole injector having a conducting injector electrode, a grid electrode, a tunnel dielectric disposed between said injector and said grid, and a retention insulator disposed between said grid and said floating gate;

a plurality of bit lines, a separate one of said plurality of bit lines coupled to said drain region of each of said plurality of nonvolatile memory cells in a same column;

a plurality of injector lines, at least one of said plurality of injector lines coupled to said conducting injector electrode of each of said plurality of nonvolatile memory cells in a same column; and

a plurality of grid lines, at least one of said plurality of grid lines coupled to said grid electrode of each of said plurality of nonvolatile memory cells in a same row.

90. A nonvolatile memory cell comprising:

a floating gate MOS transistor including;

a semiconductor body having a doping of a first type;

first and second semiconductor regions having a doping of a second type, said first and second semiconductor regions spaced apart to form a channel region in between said first and second semiconductor regions in said semiconductor body;

a floating gate disposed above said channel region in said semiconductor body;

a floating gate dielectric disposed between said floating gate and said semiconductor conductor body; and

a tunneling hole injector including:

a conducting injector electrode from which holes are emitted;

a grid electrode;

a tunnel dielectric disposed between said grid and said injector; and

a retention insulator disposed between said grid and said floating gate,

wherein charge carriers are ballistically injected from said charge injector through said retention insulator to said floating gate.

91. A nonvolatile memory cell comprising:

a floating gate MOS transistor including;

a semiconductor body having a doping of a first type;

first and second semiconductor regions having a doping of a second type, said first and second semiconductor regions spaced apart to form a channel region in between said first and second semiconductor regions in said semiconductor body;

a floating gate disposed above said channel region in said semiconductor body;

a floating gate dielectric disposed between said floating gate and said semiconductor conductor body; and

a tunneling hole injector including:

a conducting injector electrode from which holes are emitted;

a grid electrode;

a tunnel dielectric disposed between said grid and said injector; and

a retention insulator disposed between said grid and said floating gate,

wherein charge carriers are ballistically injected from said charge injector through said retention insulator to said floating gate.

92. A nonvolatile memory device comprising:

a plurality of nonvolatile memory elements arranged in a rectangular array of rows and columns, each of said plurality of nonvolatile memory elements including:

a floating gate MOS transistor having a source region and a drain region formed in a semiconductor body and spaced apart by a channel region, and a floating gate disposed above said channel region; and

a tunneling charge injector having a conducting injector electrode, a grid electrode, a tunnel dielectric disposed between said injector and said grid, and a retention insulator disposed between said grid and said floating gate;

a plurality of bit lines, a separate one of said plurality of bit lines coupled to said drain region of each of said plurality of nonvolatile memory cells in a same column;

a plurality of source lines, at least one of said plurality of source lines coupled to said source region of each of said plurality of nonvolatile memory cells in a same row;

a plurality of injector lines, at least one of said plurality of injector lines coupled to said conducting injector electrode of each of said plurality of nonvolatile memory cells in a same row; and

a plurality of grid lines, at least one of said plurality of grid lines coupled to said grid electrode of each of said plurality of nonvolatile memory cells in a same column,

wherein charge carriers are ballistically injected from said charge injector through said retention insulator to said floating gate.

93. A nonvolatile memory device comprising:

a plurality of nonvolatile memory elements arranged in a rectangular array of rows and columns, each of said plurality of nonvolatile memory elements including:

a floating gate MOS transistor having a source region and a drain region formed in a semiconductor body and spaced apart by a channel region, and a floating gate disposed above said channel region; and

a tunneling charge injector having a conducting injector electrode, a grid electrode, a tunnel dielectric disposed between said injector and said grid, and a retention insulator disposed between said grid and said floating gate;

a plurality of bit lines, a separate one of said plurality of bit lines coupled to said drain region of each of said plurality of nonvolatile memory cells in a same column;

a plurality of injector lines, at least one of said plurality of injector lines coupled to said conducting injector electrode of each of said plurality of nonvolatile memory cells in a same column; and

a plurality of grid lines, at least one of said plurality of grid lines coupled to said grid electrode of each of said plurality of nonvolatile memory cells in a same row.